System on Chip Interfaces for Low Power Design

Sanjeeb Mishra, Neeraj Kumar Singh, Vijayakrishnan Rousseau

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System on Chip Interfaces for Low Power Design provides a top-down understanding of interfaces available to SoC developers, not only the underlying protocols and architecture of each, but also how they interact and the tradeoffs involved. The book offers a common context to help understand the variety of available interfaces and make sense of technology from different vendors aligned with multiple standards. With particular emphasis on power as a factor, the authors explain how each interface performs in various usage scenarios and discuss their advantages and disadvantages. Readers learn to make educated decisions on what interfaces to use when designing systems and gain insight for innovating new/custom interfaces for a subsystem and their potential impact.

- Provides a top-down guide to SoC interfaces for memory, multimedia, sensors, display, and communication
- Explores the underlying protocols and architecture of each interface with multiple examples
- Guides through competing standards and explains how different interfaces might interact or interfere with each other
- Explains challenges in system design, validation, debugging and their impact on development

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